

IZUMI  
Appl. No. to be assigned

**AMENDMENTS TO THE ABSTRACT:**

Please replace the original Abstract with the Abstract which appears as the next page.

**ABSTRACT**

A gate insulation film (14) and a semiconductor layer (15) are laminated on a gate electrode (13); and a source electrode (17) and a drain electrode (18) are formed on the semiconductor layer (15) by having a predetermined interval between their end portions. Each of the source electrode (17) and the drain electrode (18) includes a superimposition area (17a and 18a), and at least one portion of the superimposition area (17a and 18a) has translucency. This arrangement realizes improvement of photosensitivity ( $I_p/I_d$ ) without causing complication of wiring layout or manufacturing process.